18th International Zurich Symposium on Electromagnetic Compatibility

WS-7 on Friday September 28

Robust Design of Nanometer ICs for Electromagnetic Reliability and Cosmic Radiation Immunity – MEDEA + Projects PARACHUTE and ROBIN

Workshop Chair: Thomas Steinecke (Infineon Technologies AG, Germany)
Co-Chairs: Philippe Garcin (ST Microelectronics, France), Werner John (Fraunhofer IZM, Germany)

08:00-08:10: Introduction
Thomas Steinecke (Infineon Technologies AG, Germany)

The technical objective of PARACHUTE is to initiate a paradigm change in the IC development and system application community in Europe regarding induced physical noise in nanometer circuits. The innovation proposed in this project is the development of new integral design approaches and the necessary models, algorithms and tools that take into account all levels of IC, IC-package, and high-density interconnects on PCB to allow optimization of the application in the context of a parasitic environment, especially electromagnetic interferences and particle radiation.

While applications require smaller voltages and higher frequencies, miniaturisation adds new risks of voltage distortions. To reduce design iterations and avoid unreliability or failures, ROBIN aims at preventing these effects very soon in the design flow. The project will address signal corruption in systems-in-package either at macro-level (power distribution, substrate) or micro-level (interconnect crosstalk, natural radiations). By considering manufacturing constraints, optimal trade-offs will be defined between circuit robustness and efficient use of technologies down to 45 nm.

PARACHUTE Presentations:

08:10-08:35: Pulse immunity of automotive microcontrollers
Tao Su, Markus Unger, Thomas Steinecke (Infineon Technologies AG, Germany)

Pulse immunity of highly integrated ICs has not been investigated systematically yet because of lacking a well-defined test setup like it is available e.g. for electromagnetic emission and RF susceptibility. A systematic approach for pulse disturbance studies will be given in the presentation. Main goal is to stick to realistic pulse stress values as they appear when applying ISO pulses to an electronic system. Local pulses remaining from ISO pulses at microcontroller IC pins have been categorized with respect to typical passive and active coupling paths. Test setups and intermediate results of the study are described during the presentation. Differences and analogies over several technology generations of microcontrollers are explained.

08:35-09:00: Rapid assessment of electromagnetic susceptibility of Integrated Circuits
Johan Loeckx, Georges Gielen (Katholieke Universiteit Leuven, Belgium)

The design of the circuit on the chip itself determines the immunity of an IC. In addition, process variations, the design of the PCB, the test setup and the parasitic behaviour of SMD components are important factors that can not be neglected while considering IC susceptibility. A fast methodology based is proposed that allows a quick assessment of the electromagnetic susceptibility of a chip. It takes into account models for all these effects, while avoiding long and tedious simulations. This allows designers to rapidly investigate EM susceptibility and pinpoint potential problems at design stage of the IC.

09:00-09:25: Introduction to advanced EMI near-field scanning
Adam Tankielun (Fraunhofer IZM, University of Paderborn, Germany), Goeran Schubert (Continental Automotive Systems, Germany)

Demand on a source reconstruction with a high spatial resolution as well as radiation prediction provoked by an arbitrary test object emitting periodic radiation, e.g. mixed analog-digital system, motivates further development of EMI near-field scanner. The workshop presents and discusses an overview of some recent advances and challenges on the subject. Selected topics include: (1) New requirements for EMI near-field scanner; (2) Differences between advanced and standard EMI scanning techniques; (3) Overview of scanner applications; (4) Overview of measurement architectures; (5) Near-field data post-processing techniques; (6) Limitations of the EMI scanner.

09:25-09:50: EMC IC modelling framework IEC 62433
Remco de Jager (NXP, The Netherlands)

To forecast Power Integrity (PI), Signal Integrity (SI) and RF emission behaviour of new IC designs in their application, all levels of design; dies, package, PCB must be linked to enable simulation and analysis. A simplified model for the excitation is required digital cores and I/Os as well as the interfaces through the package onto the PCB. In IEC 62433, a new modelling framework has been defined which also allows the inclusion of existing IBIS and ICEM models as well as S-parameter models used for the conductive or radiated coupling path. The concept as well as some intermediate results will be presented.

09:50-10:15: Cosmic Radiation Induced Effects in VDSM ICs
Lorena Anghel (TIMA), Dan Alexandrescu (iRoC)

Due to the significant reduction of the reliability of very deep submicron (VDSM) ICs versus various internal and external sources of noise, a significant problem is caused by the sensitivity of ICs versus energetic particles, such as heavy ions, protons and even atmospheric neutrons. Chip manufacturers and system integrators for networking, aeronautical and space applications are interested in evaluating the sensitivity of the devices against these perturbations. Radiation testing can offer real-life data about the behaviour of the circuits and laser testing is a useful analysis tool. Following the phenomenon from the impact of the particle (physical aspects) through circuit problems (electrical propagation of the fault through the logic network) and arriving at the system level (software/program errors), a large panoply of tools and methods can be used, such as 3D, electrical, gate-level and RTL simulations and FPGA emulation. We will present an ensemble of methodologies that aims at providing the IC designer with necessary tools for a better comprehension of the radiation-induced effects in VDSM ICs.

10:15-10:30: Coffee break

ROBIN Presentations:

10:30-10:55: Intra-block and inter-block parasitic couplings
Jean-Paul Morin (ST Microelectronics, France)

This talk is devoted to accuracy improvement of post-layout extraction by an in-depth analysis of the impact of RLCK parasitics on performances. As a first step, sophisticated techniques were proposed, aimed at reducing the size of extracted netlists. This makes it possible for designers to perform simulations at a reasonable speed. Then, modeling the System in Package (SiP) appeared as a key issue for teams designing high speed digital or analog/RF circuits. So a second phase addressed this type of modeling. In parallel with actions on very accurate modeling based on 3D solvers, simplified models and flows are under construction, used by IC designers in standard flows. This requires adapting or tuning IC extractors to SiP technologies (geometries, shapes...). In addition, another source of noise onboard ICs is the power grid itself. To alleviate this problem, new flows were qualified, in cooperation with EDA Vendors, to provide accurate modeling and visualization of grid impact on signal quality.

10:55-11:20: Analog RF simulations including the parasitic behaviour of the power supply grid
Martin Unterweissacher (University of Technology Graz, Austria), Thomas Brandtner (Infineon Technologies AG, Austria)

The parasitic behaviour of on-chip power distribution networks has to be considered during the design of sensitive analog circuit blocks. Pre-layout power grid models are introduced that enable circuit designers to simulate and investigate in power grid configurations before effort has to be spent for layouts. Parasitic inductances are also included in the power grid models to allow valid RF circuit simulations.

11:20-11:45: Extended chip-package cosimulation (ECOS)
Markus Pistauer (CISC Semiconductor Design+Consulting GmbH, Austria)

As clock rates, bus widths and speeds have been significantly increased using sub-nanometer technologies, packaging and interconnects will have significant importance and in some cases actually limit or define the system, where silicon performance is usually found to be the gating factor. It will be the case that packaging and interconnects dominate electrical considerations at some point as connects/networks become more and more prominent. Further on due to the increasingly important lateral capacitance components in the interconnect, cross-talk has become a key signal-integrity effect. In this work a mixed-signal co-design simulation flow is presented that will consider package parasitics coming from package extraction in state of the art design environments.

11:45-12:10: Power Integrity in System-on-Chip (SoC)
Paul van de Wiel, Maurice Meijer (NXP, The Netherlands)

The decreasing feature sizes in deep sub-micron technologies enable increased packing densities with more functional blocks on an SoC. Along with the feature sizes, the supply and threshold voltages scale accordingly, which cause a reduction of the noise margins. On the opposite, the switching current and switching speed increase, generating more supply noise, and substrate noise. As a consequence, to achieve correct operation of the combined analogue, radio frequency (RF) blocks and digital blocks becomes very difficult.
In this work a design strategy for an optimal power grid is investigated to minimize IR-drop and supply bounce. The design strategy is based on physical insight, gained with newly developed macro models.